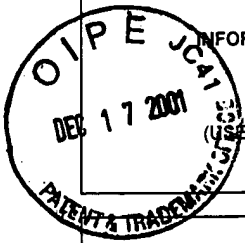


Paper #4

4



FORM PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. ARC.015A	APPLICATION NO. 09/808,469
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (USE SEVERAL SHEETS IF NECESSARY)		APPLICANT Peter Warnes	
		FILING DATE March 14, 2001	GROUP 2123

U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
<i>MS</i>	1	5,463,746	10/31/95	Brodnax, et al.			
<i>MS</i>	2	5,748,650	05/05/98	Blaker, et al.			
<i>MS</i>	3	5,764,994	06/09/98	David John Craft			
<i>MS</i>	4	5,794,010	08/11/98	Worrell, et al.			
<i>MS</i>	5	5,867,681	02/02/99	Worrell, et al.			
<i>MS</i>	6	5,896,519	04/20/99	Frank Worrell			
<i>MS</i>	7	5,901,310	05/04/99	Rahman, et al.			
<i>MS</i>	8	5,905,893	05/18/99	Frank Worrell			
<i>MS</i>	9	6,195,743	02/27/01	Elmootazbellah Elnozahy			
<i>MS</i>	10	6,233,674	05/15/01	Elmootazbellah Elnozahy			
<i>MS</i>	11	6,237,080	05/22/01	Rauno Makinen			
<i>MS</i>	12	6,263,429	07/17/01	Charles P. Siska			
<i>MS</i>	13	6,268,809	07/31/01	Akira Saito			
<i>MS</i>	14	6,275,921	08/14/01	Iwata, et al.			

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FOREIGN PATENT DOCUMENTS								
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)	
<i>MS</i>	15	Lefugry, Charles, et al. (1999) "Evaluation of a High Performance Code Compression Method," IEEE - Proceedings of Micro 32 (consisting of 10 pages).
<i>MS</i>	16	Application Serial No. 09/418,663 entitled "Method and Apparatus for Managing the Configuration and Functionality of a Semiconductor Design," filed October 14, 1999 - Attorney Docket No. ARC.001A

EXAMINER <i>Sherry Shotton</i>	DATE CONSIDERED 4.19.04
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U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
<i>MA</i>	17	5,819,058	10/06/98	Miller, et al.			
<i>MA</i>	18	5,848,255	12/08/98	Yoshikazu Kondo			

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FOREIGN PATENT DOCUMENTS								
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
<i>MA</i>	19	EP 0 843 253 A1	May 1998	Europe				
<i>MA</i>	20	WO 00/29938	May 2000	PCT				

EXAMINER INITIAL	OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)	

EXAMINER <i>May</i>	DATE CONSIDERED <i>4.19.2004</i>
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT		APPLICANT Peter Warnes	
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
<i>MX</i>	21	5,812,416	09/22/98	Gupte, et al.			
<i>MX</i>	22	5,884,057	03/16/99	Blomgren, et al.			

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
<i>MX</i>	23	EP 1 050 798 A1	May 1999	Europe				

OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)

EXAMINER INITIAL		
<i>MX</i>	24	Berekovic, et al., (Oct. 1998), "A Core Generator for Fully Synthesizable and Highly Parameterizable RISC-Cores for System-On-Chip Designs," IEEE Workshop on Signal Processing Systems: SIPS. Design and Implementation, Pages 561-568. XP002137267
<i>MX</i>	25	Karl Gutttag (March 1983), "µP's on-chip macrocode extends instruction set," Electronic Design, Vol. 31, No. 5, Pages 157-161
<i>MX</i>	26	Dolle, et al., (July 1997), "A 32-b RISC/DSP Microprocessor with Reduced Complexity," IEEE Journal of Solid-State Circuits, IEEE Inc., New York, Vol. 32, No. 7, Pages 1056-1066. XP000729365

EXAMINER <i>My Station</i>	DATE CONSIDERED <i>4.19.2004</i>
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